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Title: Storage Control Device

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FIG. 1

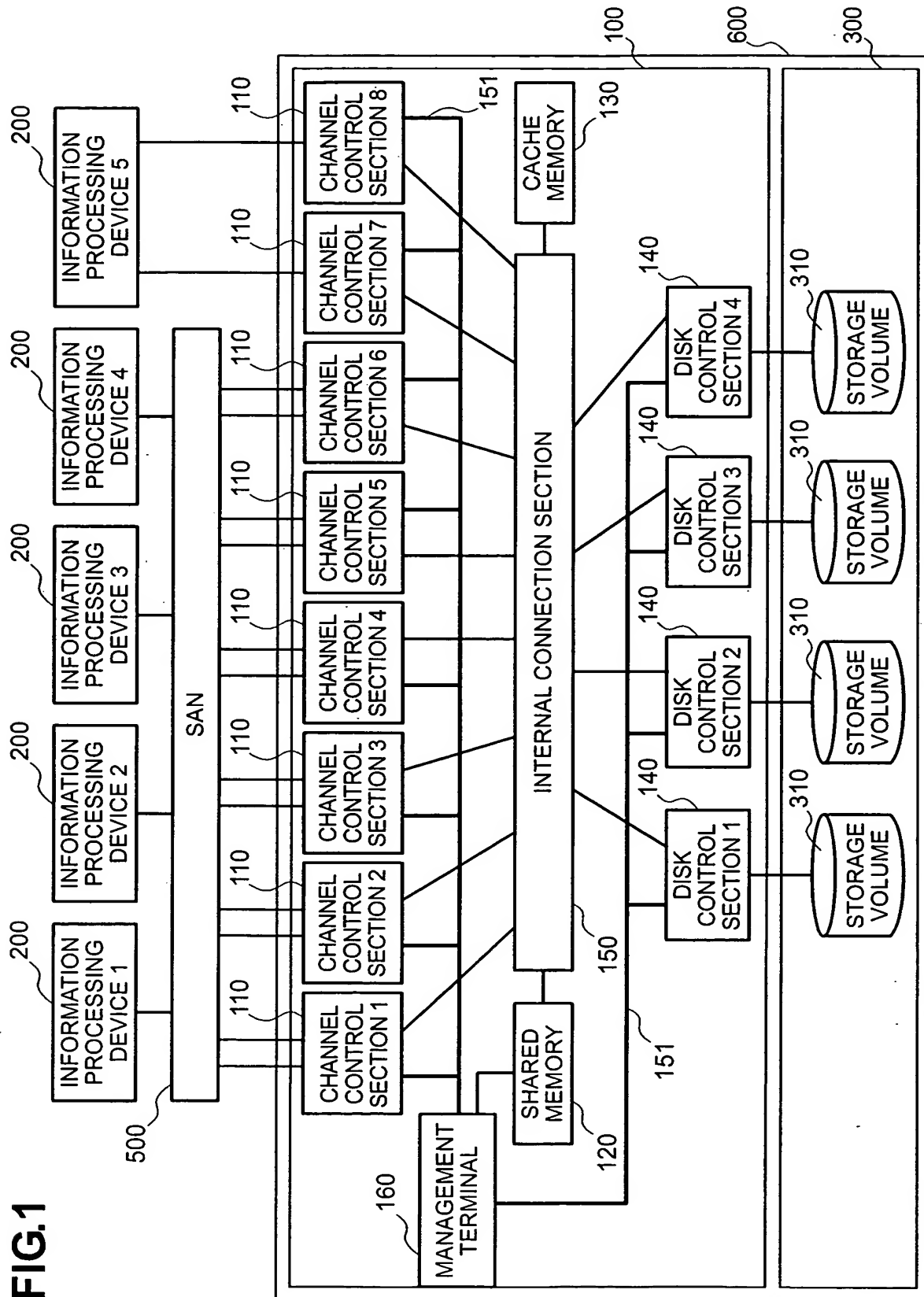
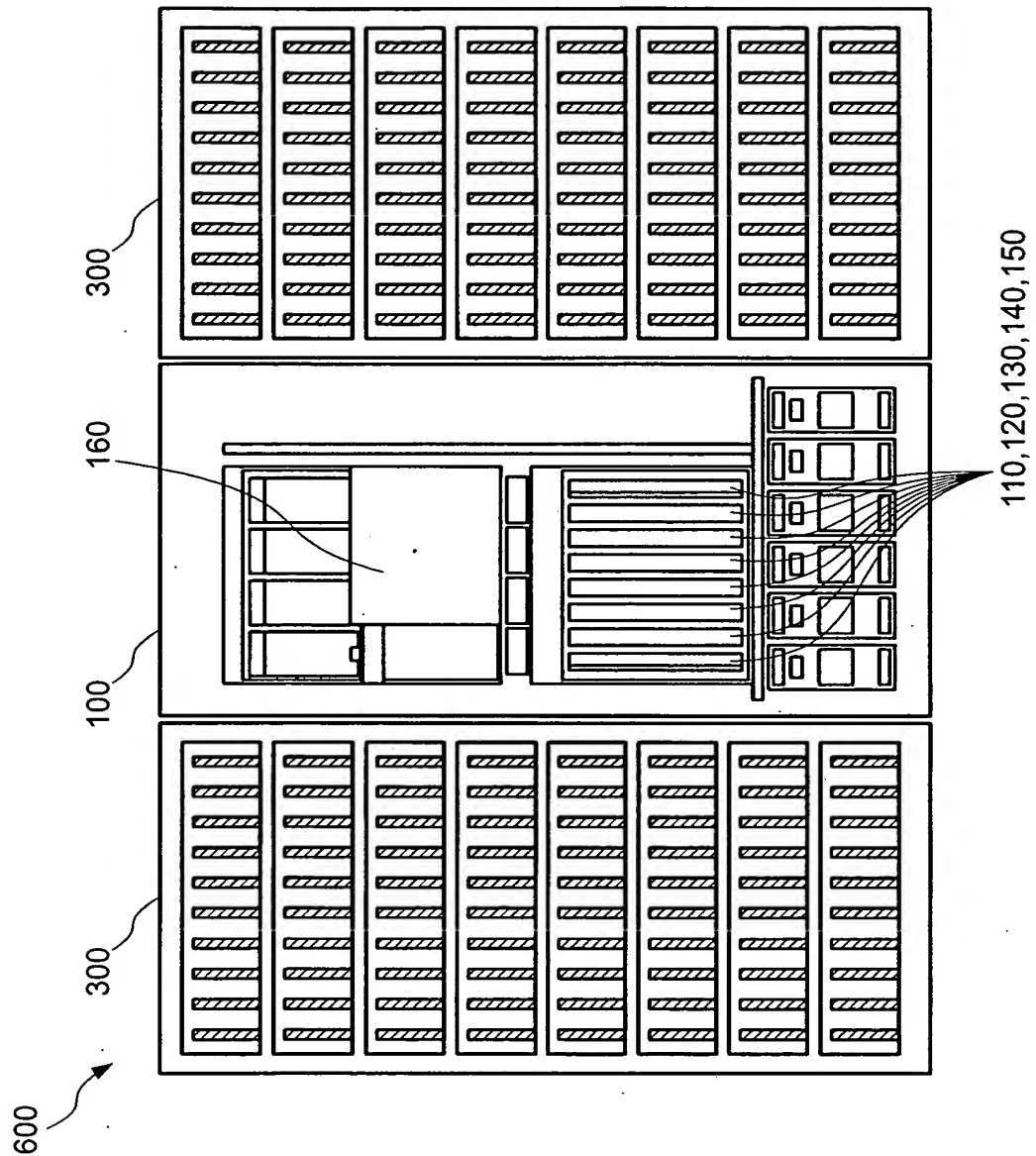


FIG.2



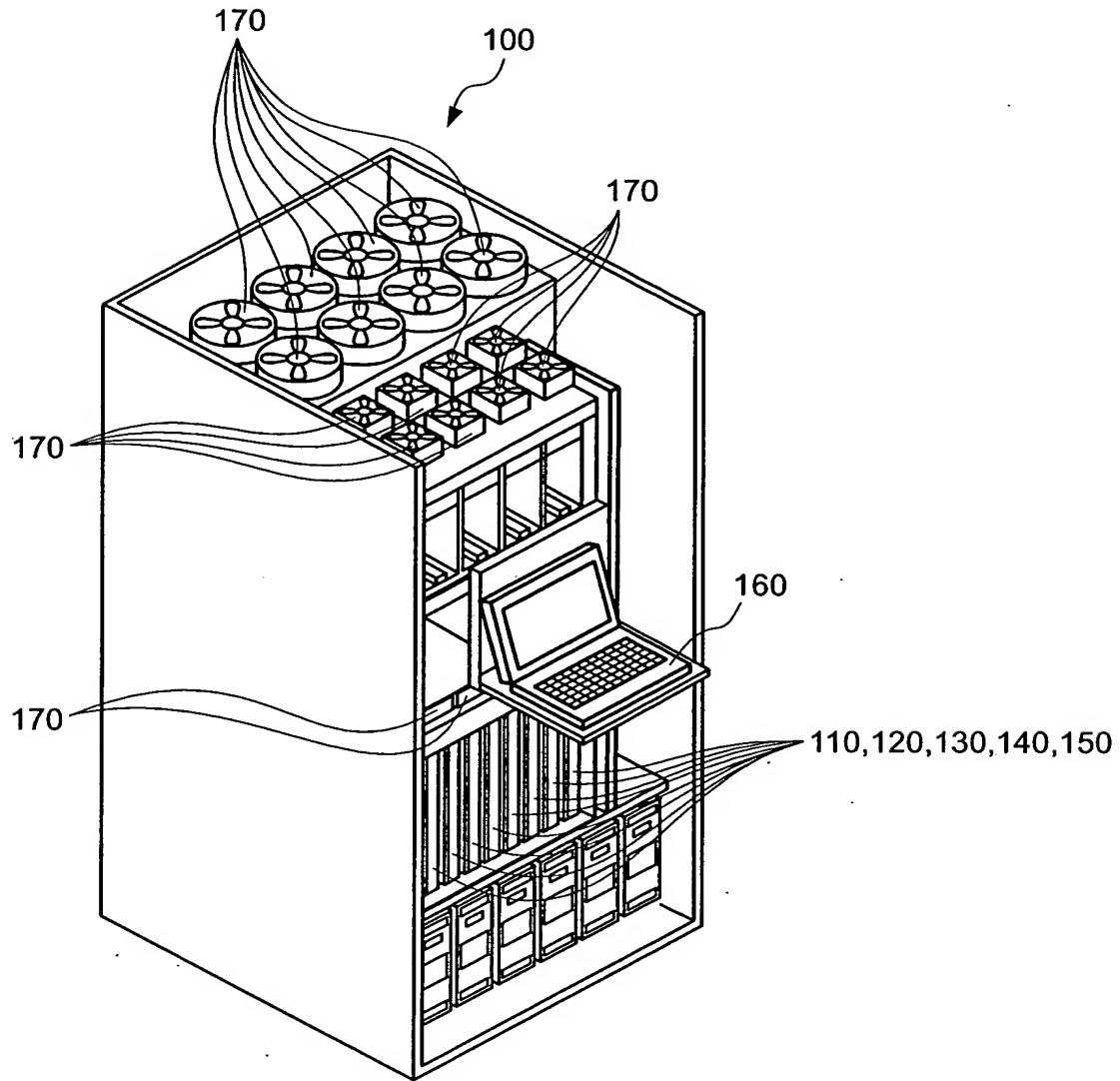
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FIG.3

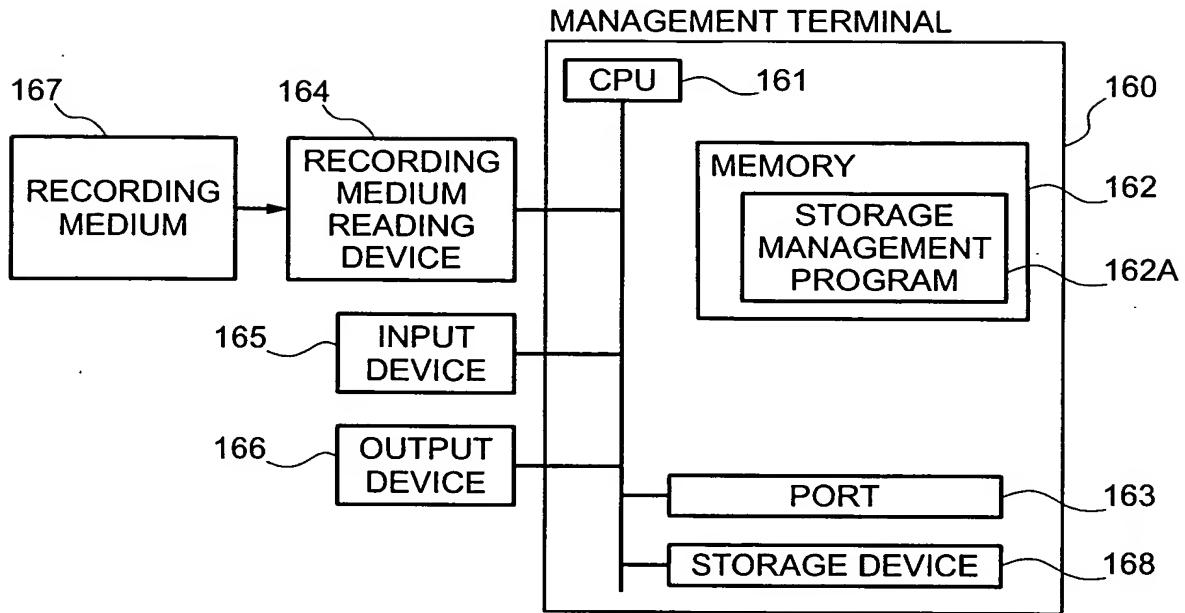
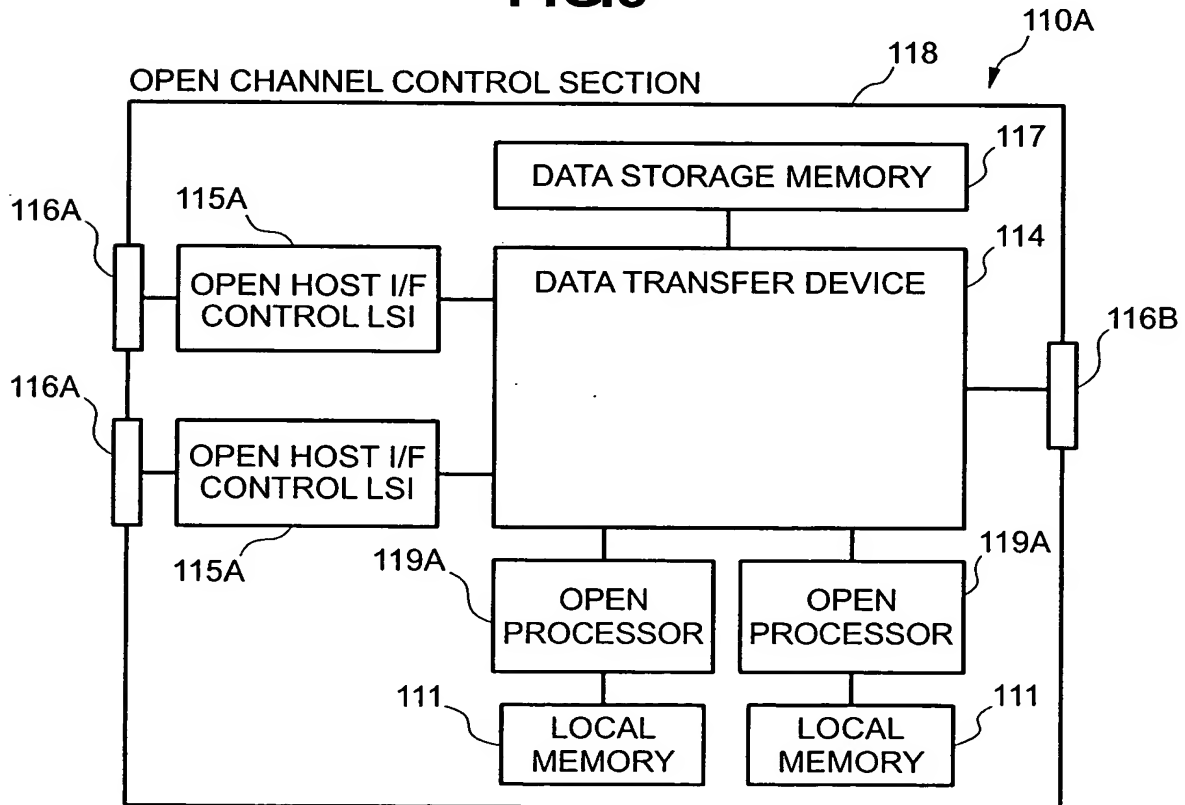


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FIG.4**FIG.5**

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FIG.6

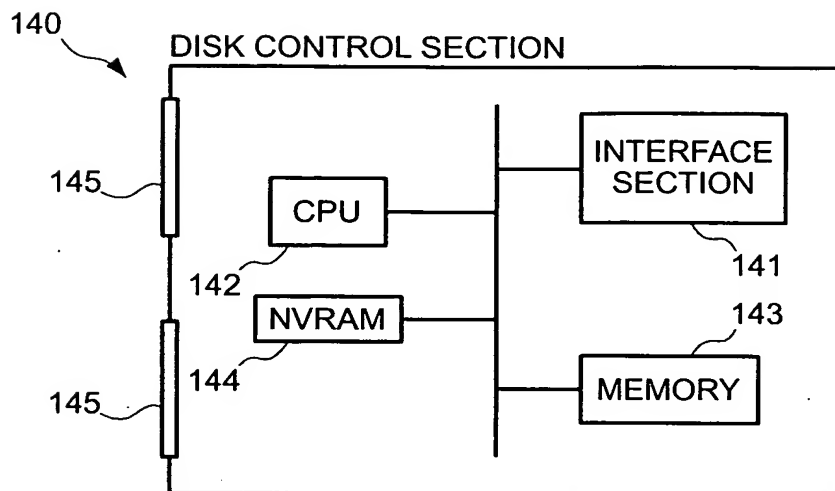


FIG.7

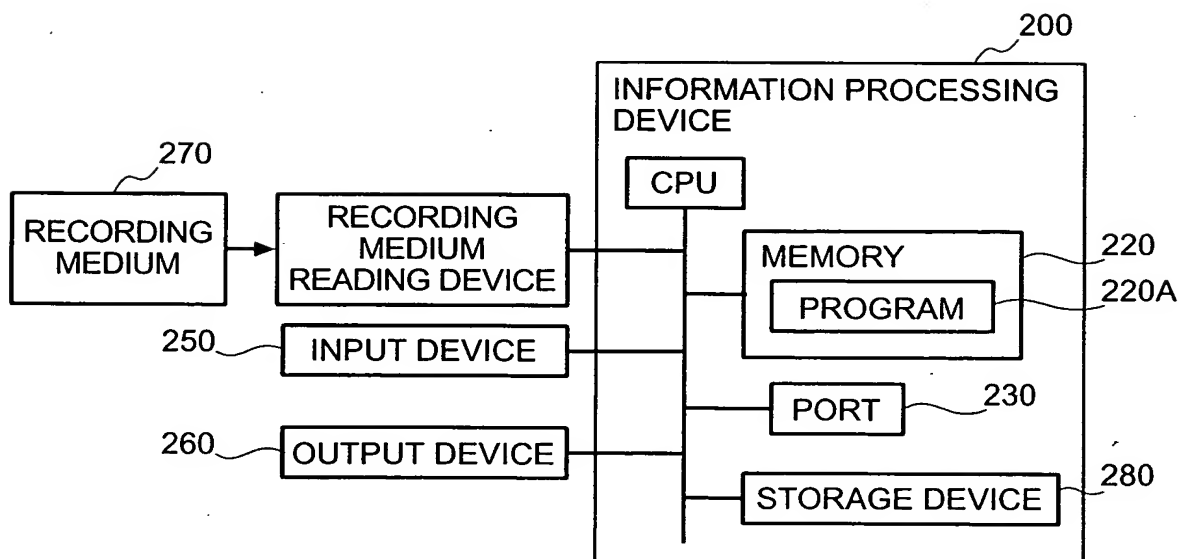


FIG. 8

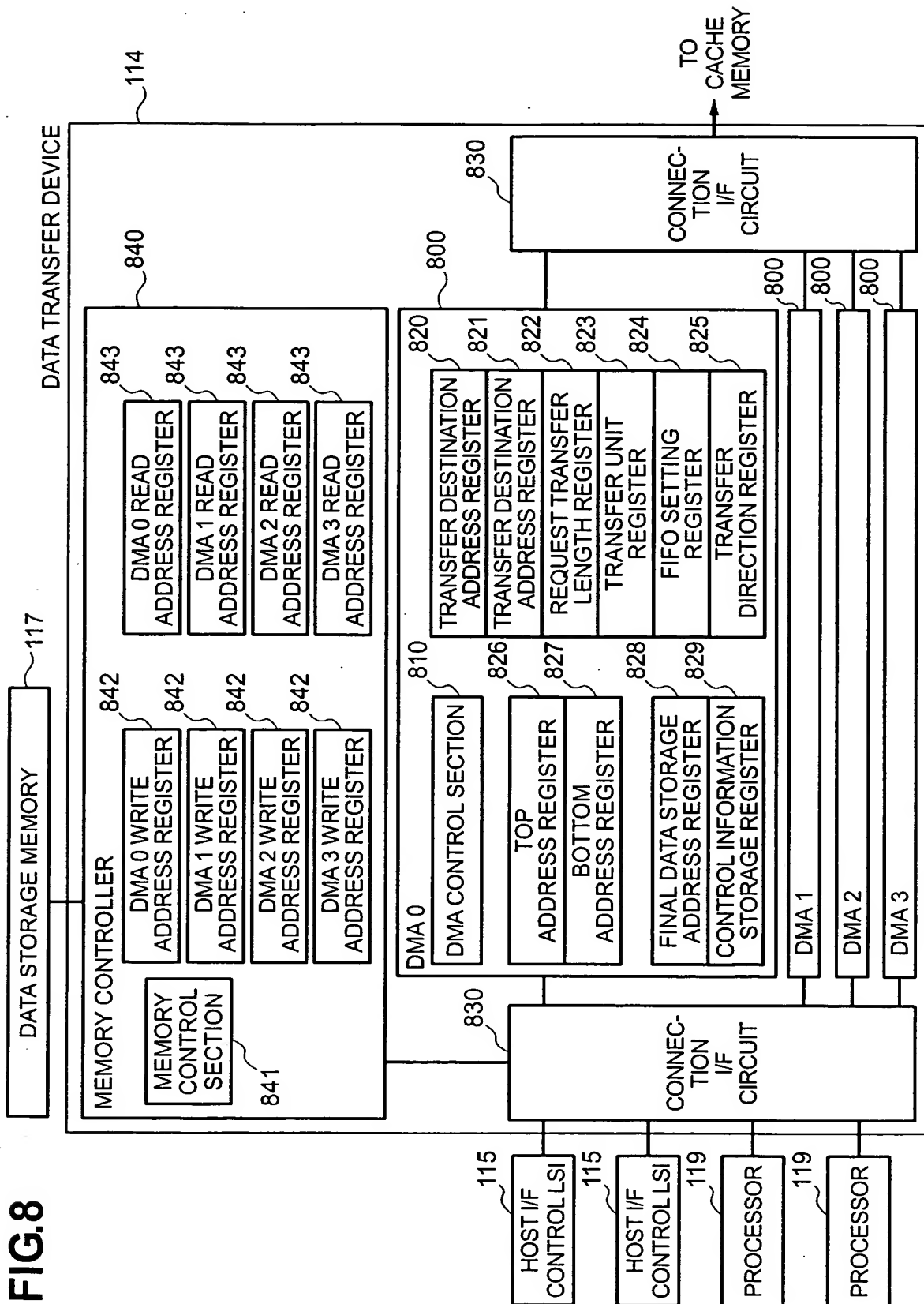
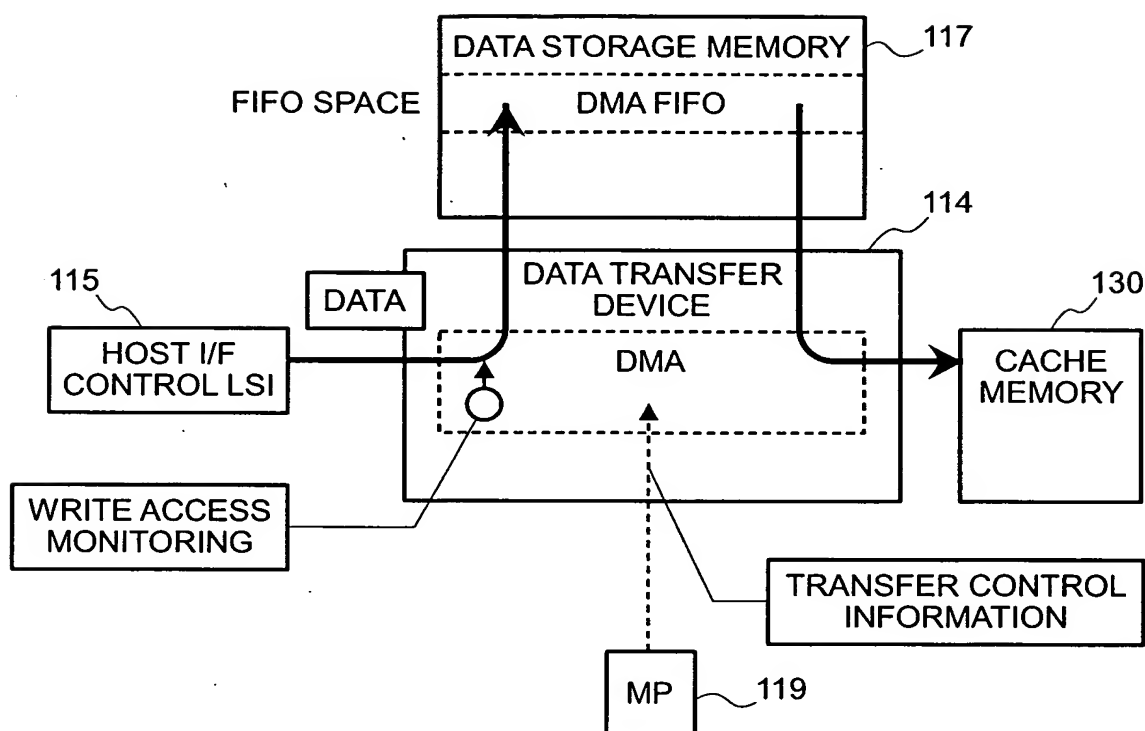


FIG.9

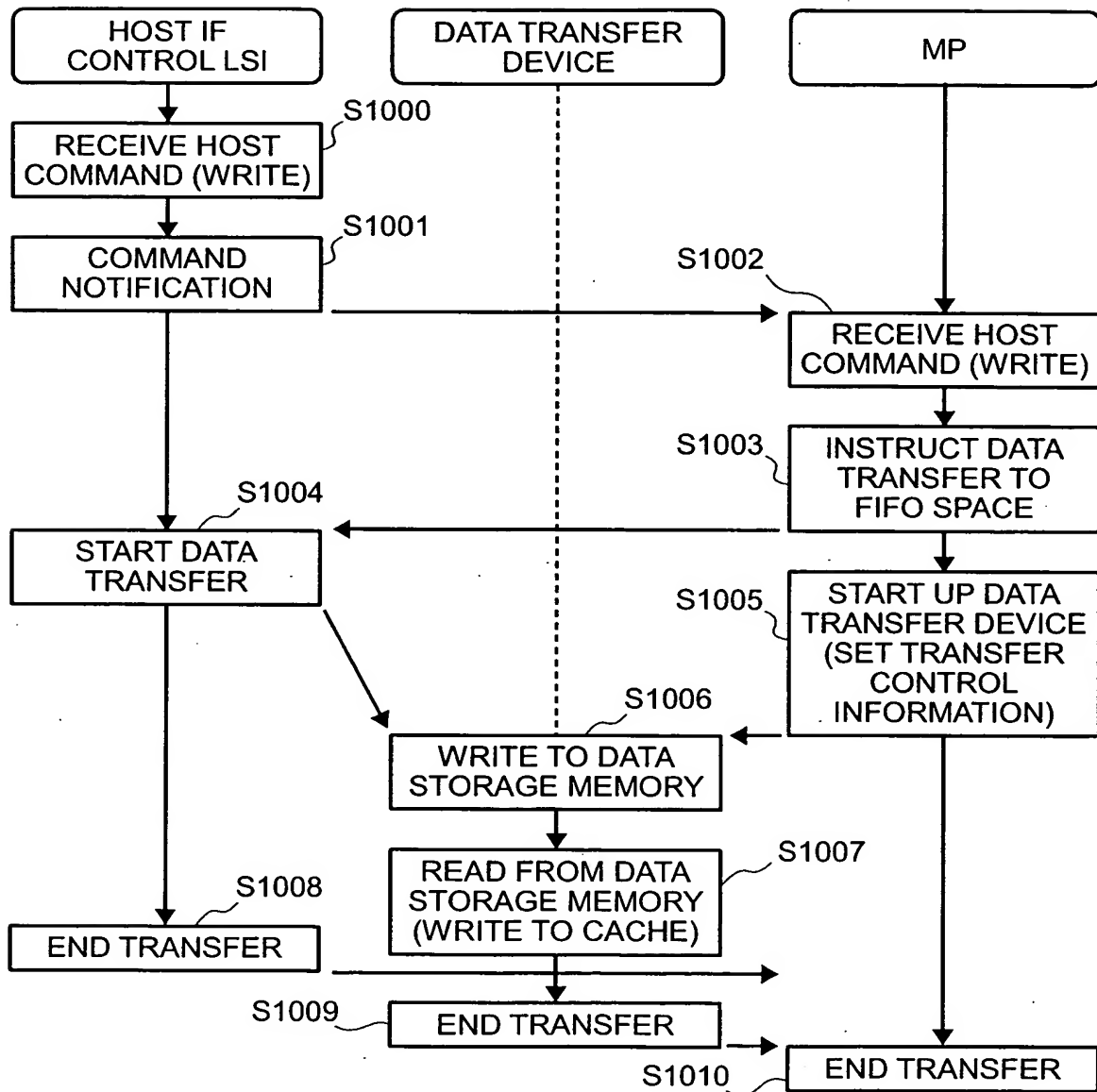
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FIG.10



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FIG.11

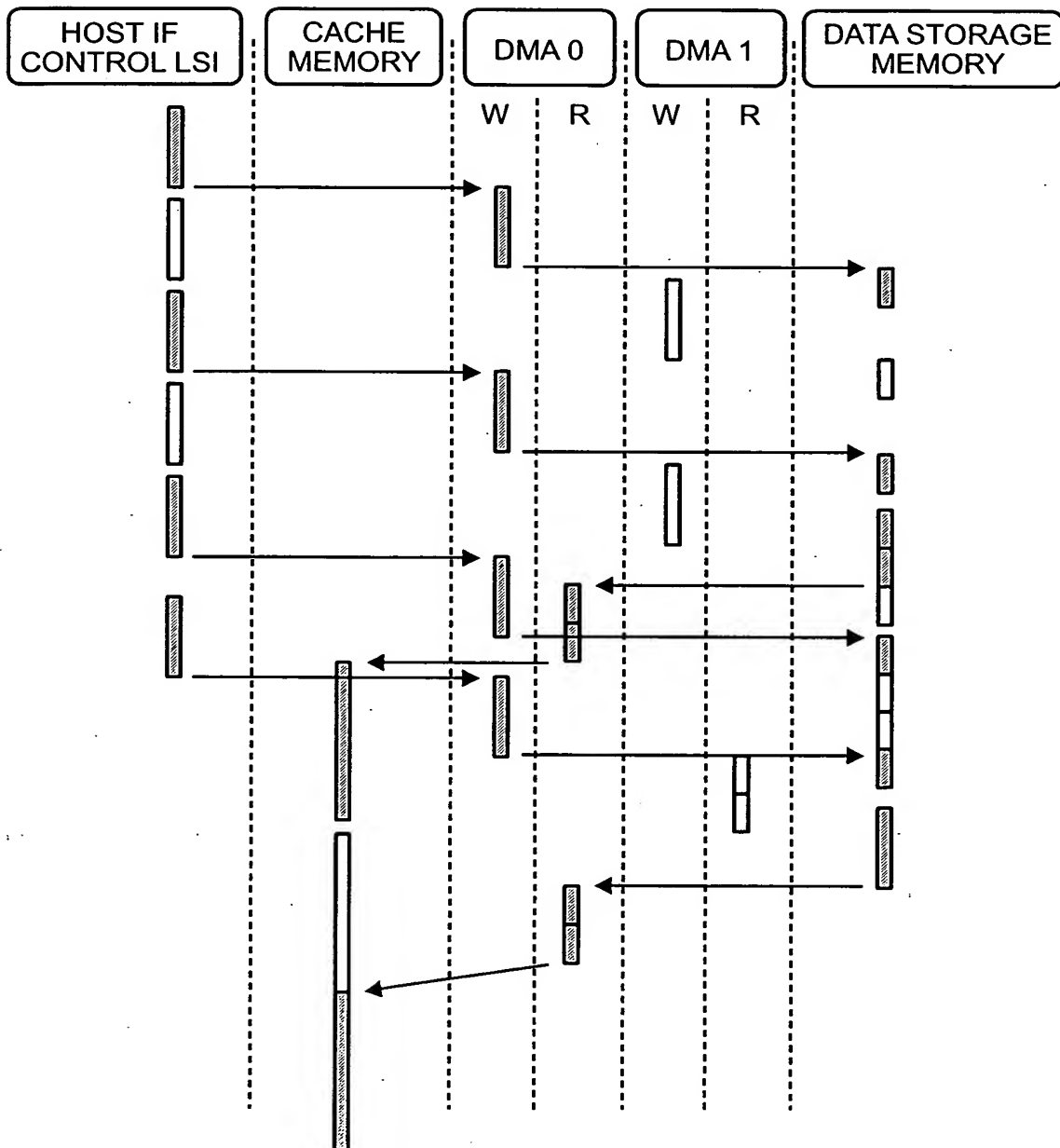
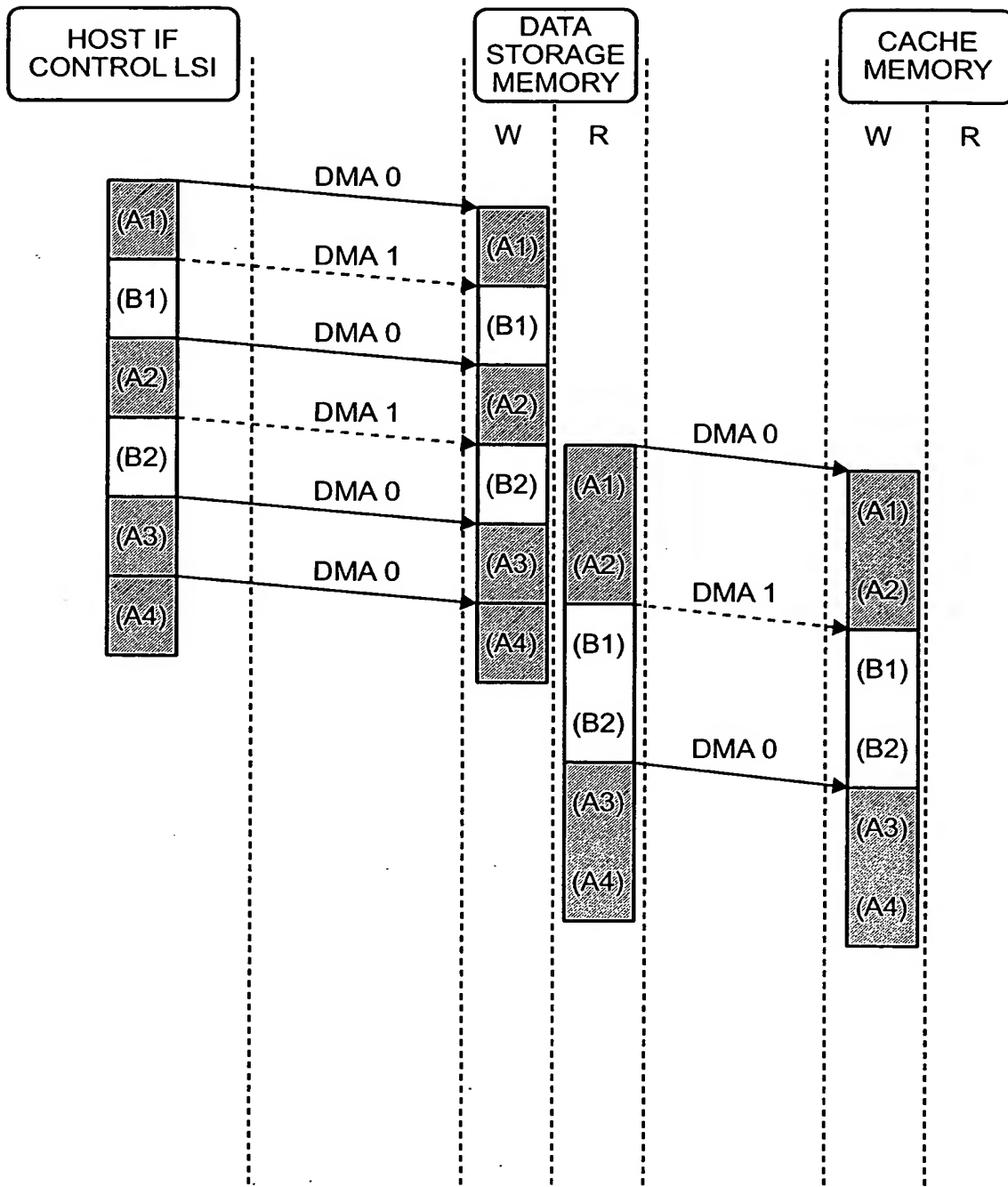


FIG.12

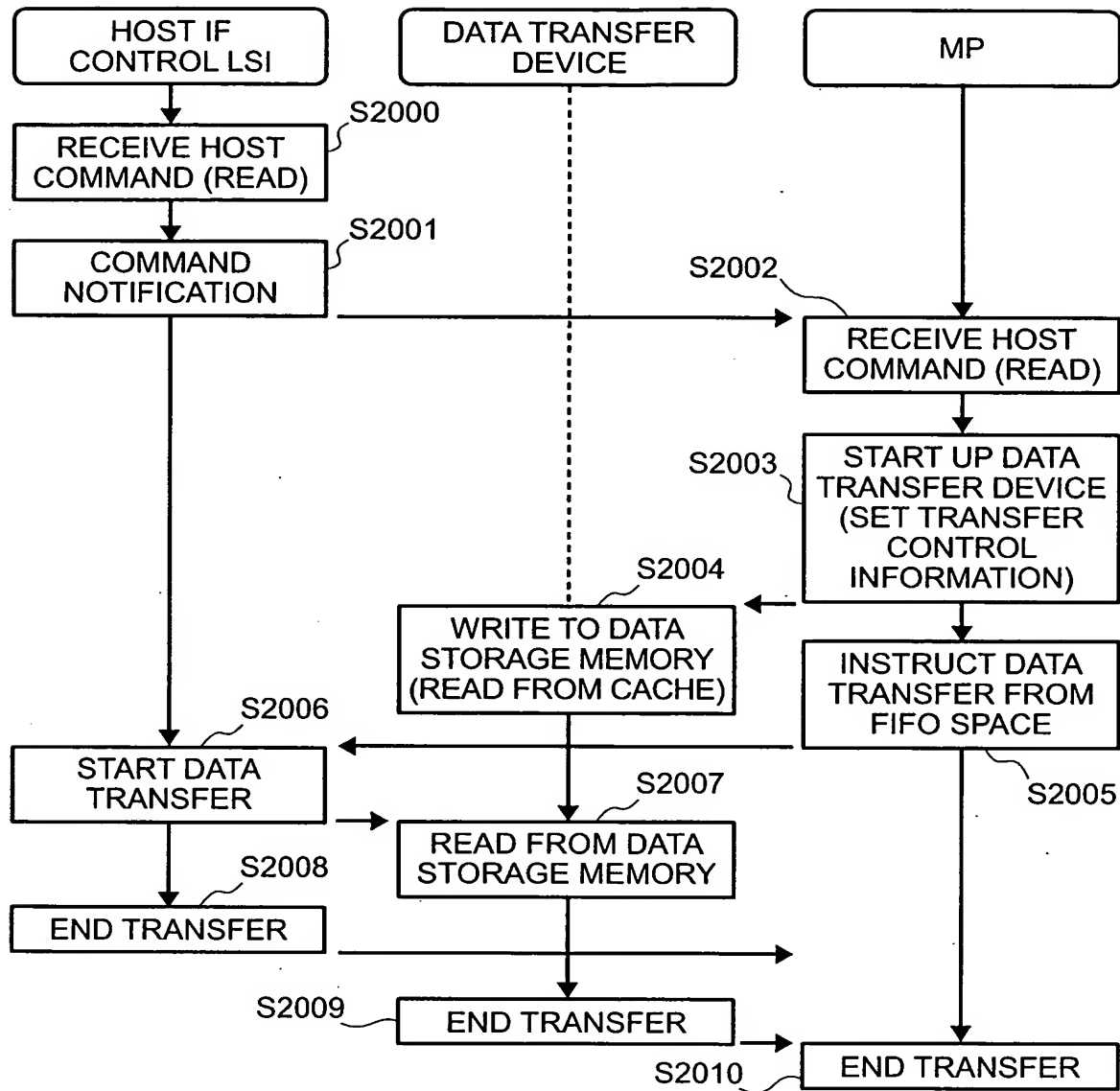
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FIG.13



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FIG.14

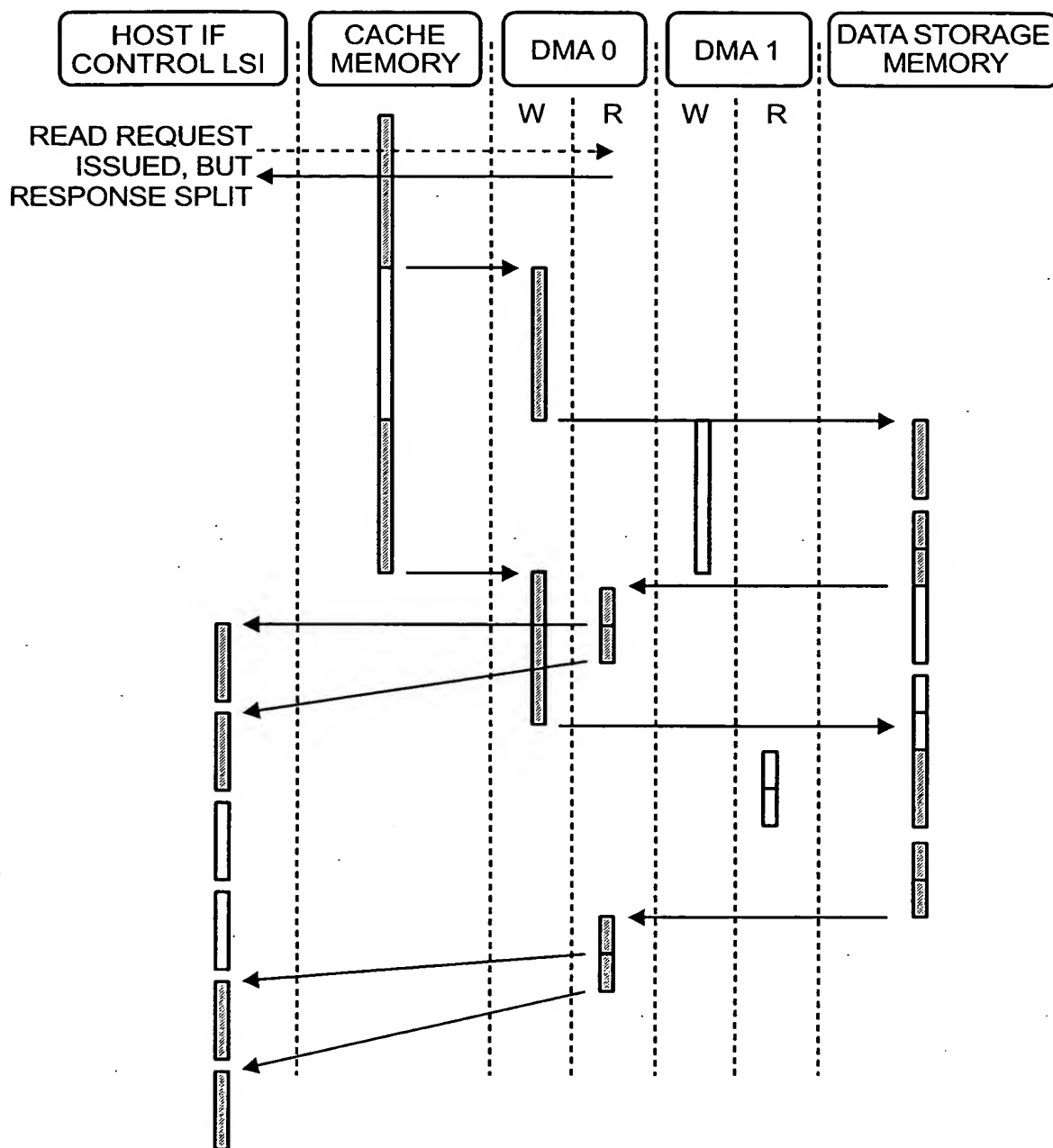
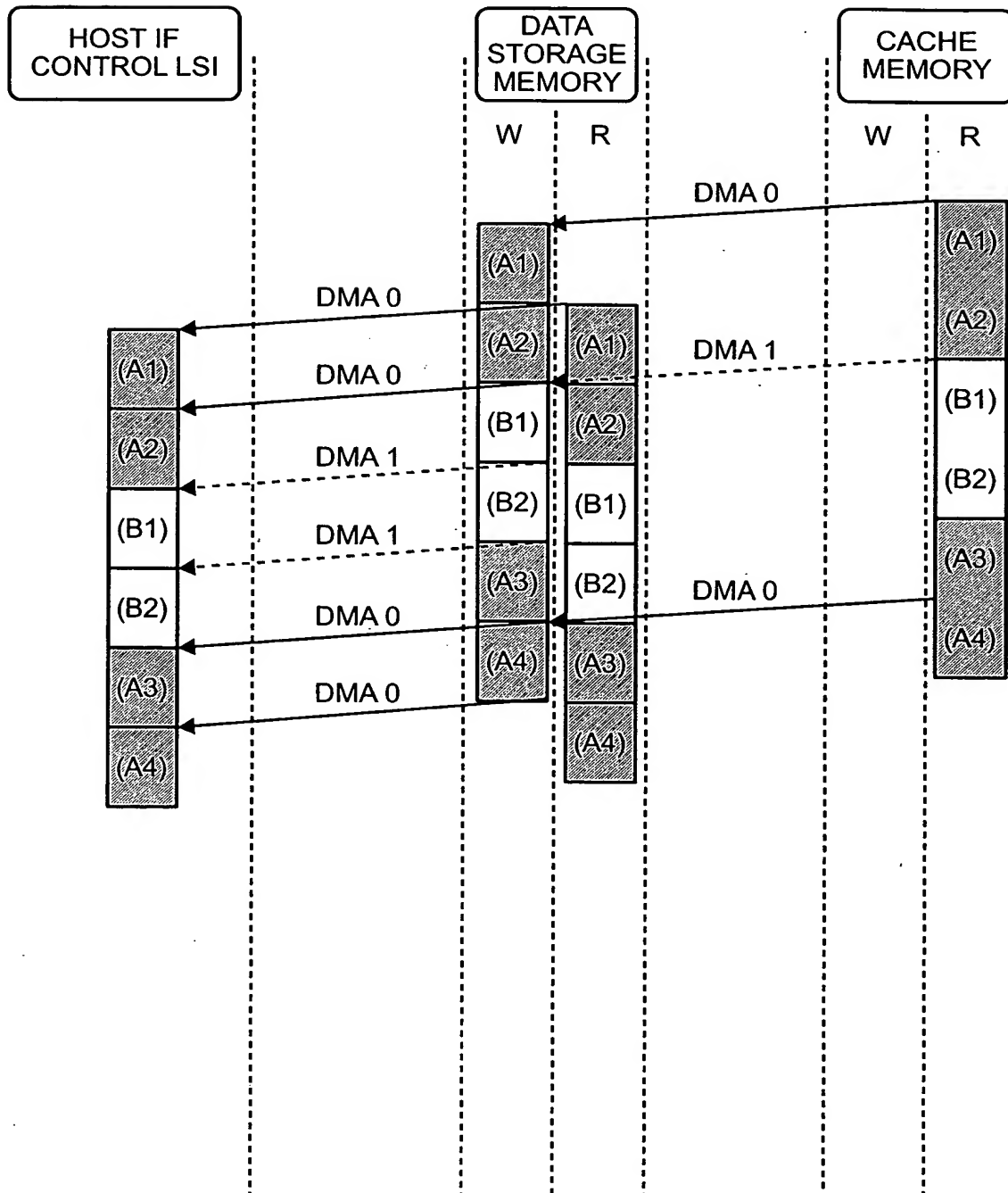


FIG.15



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DATA STORAGE MEMORY 117

FIFO SPACE 0

FIFO SPACE 1

DMA FIFO 0

DMA FIFO 1

DATA TRANSFER DEVICE 114

DMA

CACHE MEMORY 130

HOST I/F CONTROL LSI 115

DATA

MONITOR WRITE ACCESS

MP 119

5) TERMINATION REPORT

2) FIFO 0 STARTED UP BY TRANSFER CONTROL INFORMATION

6) NEXT, FIFO 1 IS STARTED UP

3) ACCESS ONLY PERMITTED TO FIFO SPACE 0

4) SIMULTANEOUSLY MONITOR WRITE ACCESS, AND [ILLEG.??] DATA

1) TRANSFER OF SEVERAL I/O TO THE RESPECTIVE FIFO SPACES IS INSTRUCTED. IN THIS DIAGRAM, START UP OF THE TWO I/O IN THE ORDER FIFO 0, FIFO 1 IS INSTRUCTED.

THE LSI'S START UP IN THE SAME ORDER THAT THE TWO I/O WERE STARTED UP, BUT A RETRY OPERATION IS EXECUTED FOR FIFO 1 UNTIL THE DMA PERMITS ACCESS TO FIFO 1.

THE LSIS START UP IN THE SAME ORDER THAT THE TWO I/O WERE STARTED UP, BUT A RETRY OPERATION IS EXECUTED FOR FIFO 1 UNTIL THE DMA PERMITS ACCESS TO FIFO 1.

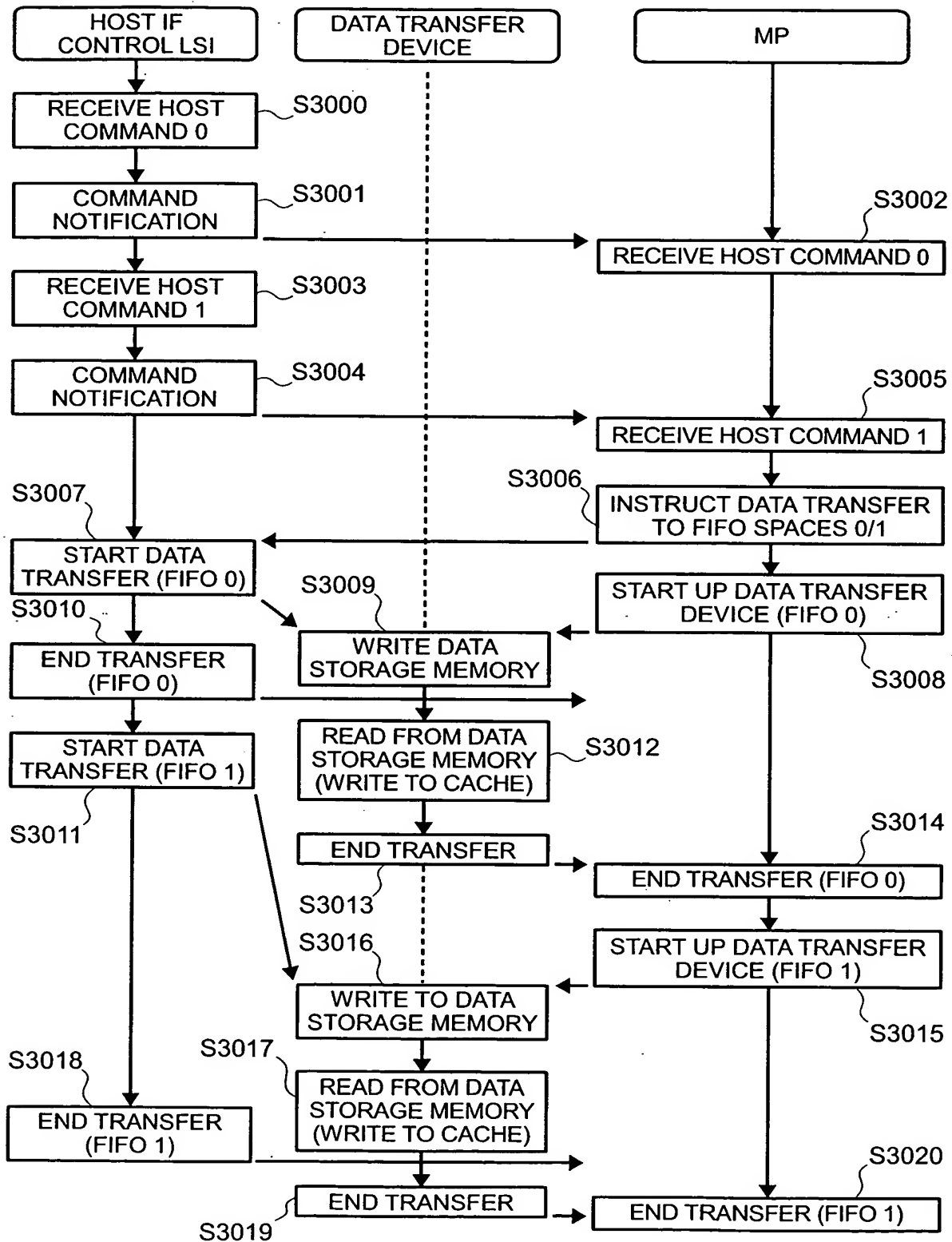
1) TRANSFER OF SEVERAL I/O TO THE RESPECTIVE FIFO SPACES IS INSTRUCTED. IN THIS DIAGRAM, START UP OF THE TWO I/O IN THE ORDER FIFO 0, FIFO 1 IS INSTRUCTED.

3) ACCESS ONLY PERMITTED TO FIFO
SPACE 0

4) SIMULTANEOUSLY MONITOR WRITE
ACCESS, AND [ILLEG.??] DATA

5) TERMINATION REPORT

2) FIFO 0 STARTED UP BY TRANSFER
CONTROL INFORMATION
6) NEXT, FIFO 1 IS STARTED UP

FIG.17

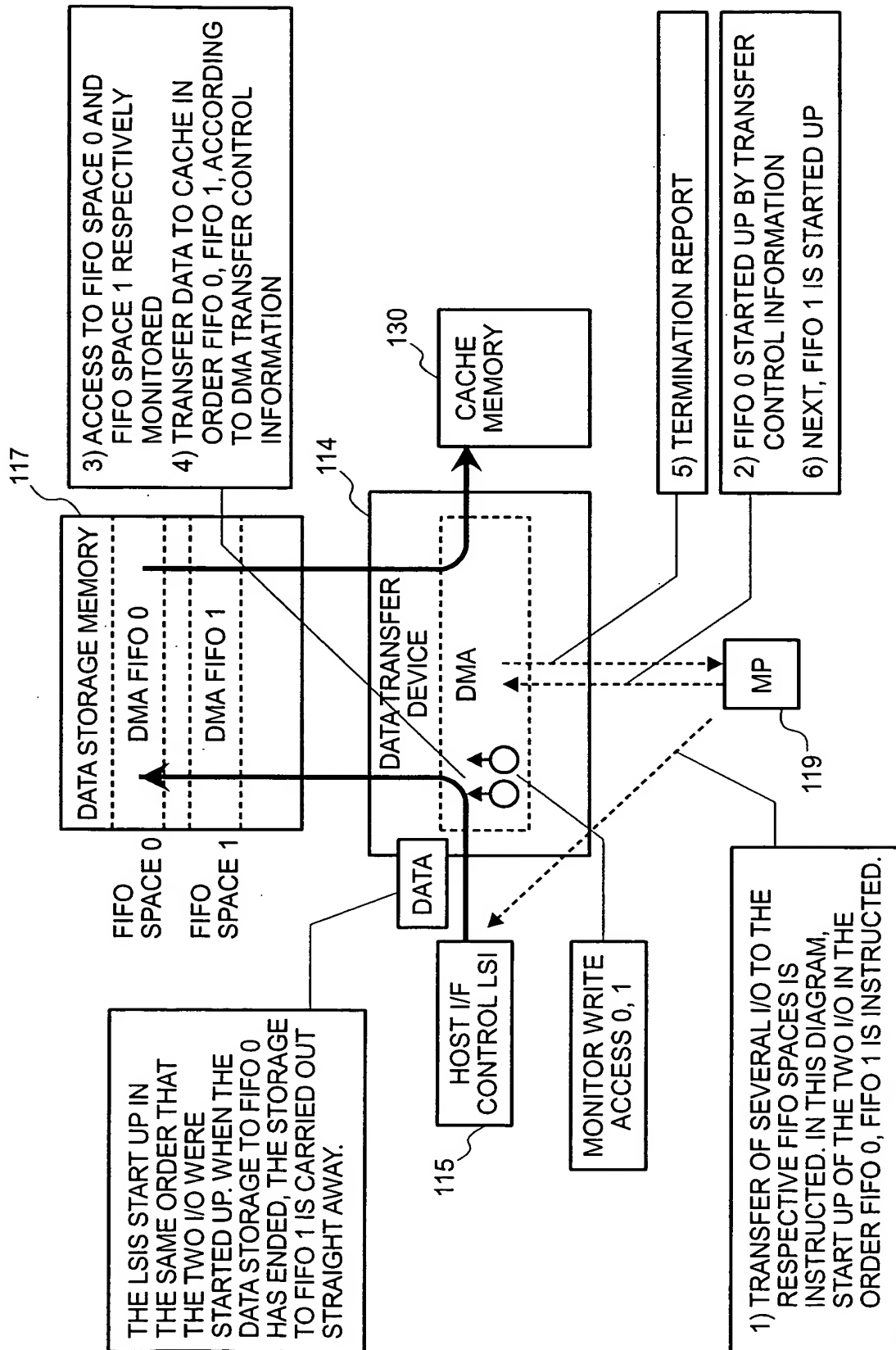
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FIG. 18



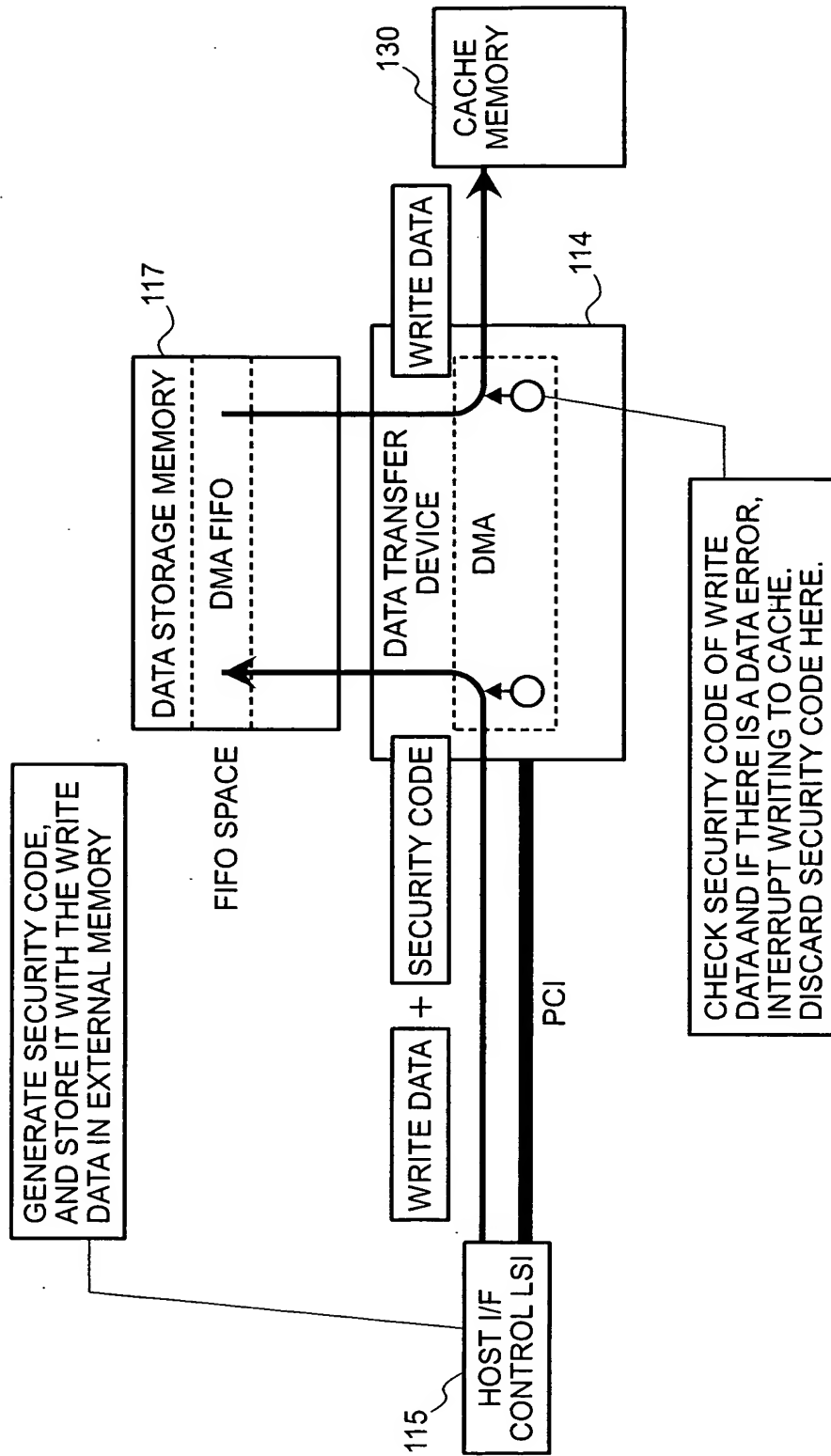
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FIG.19



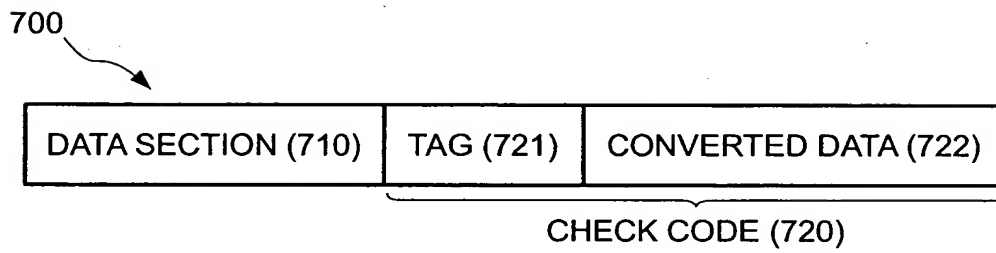
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FIG.20

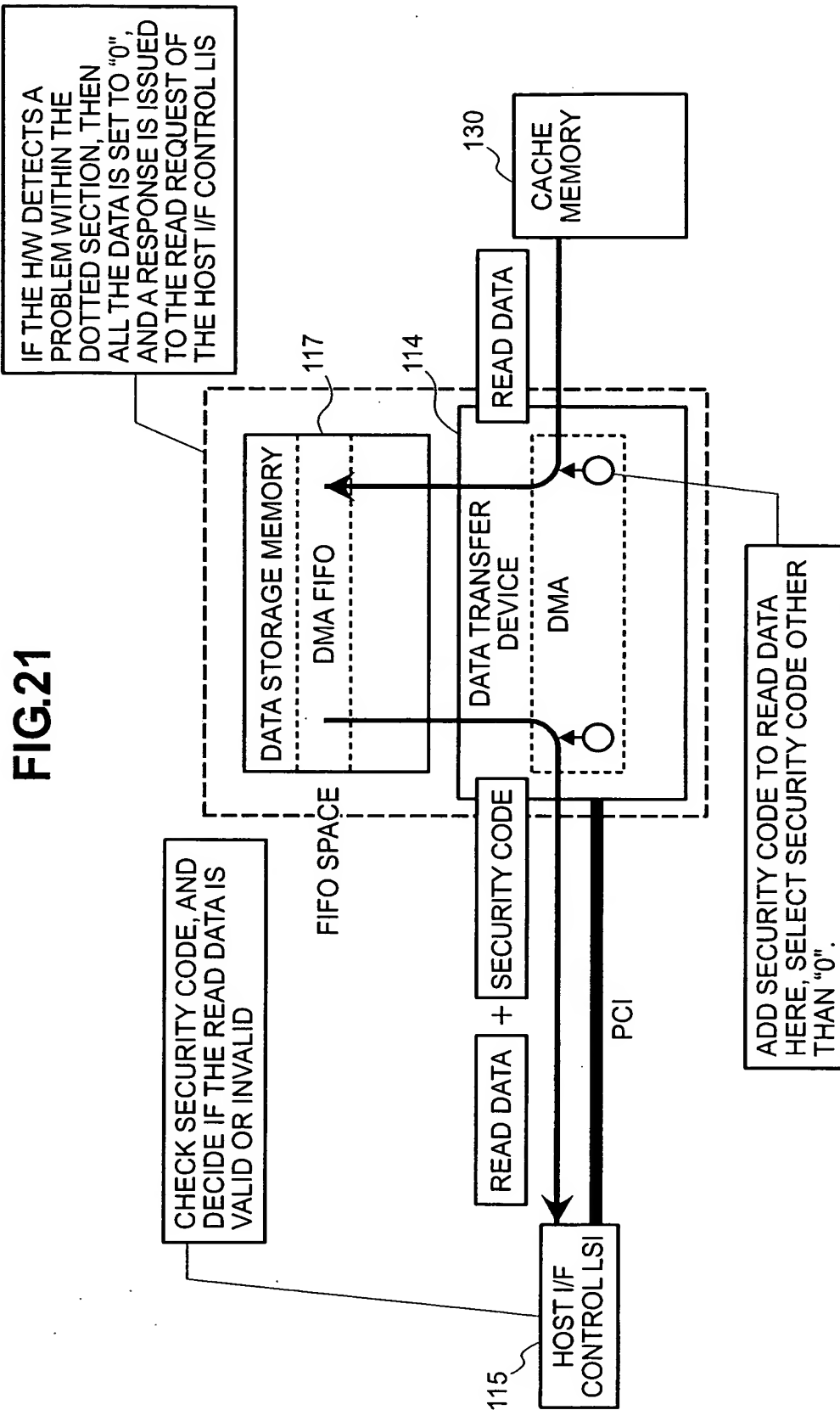


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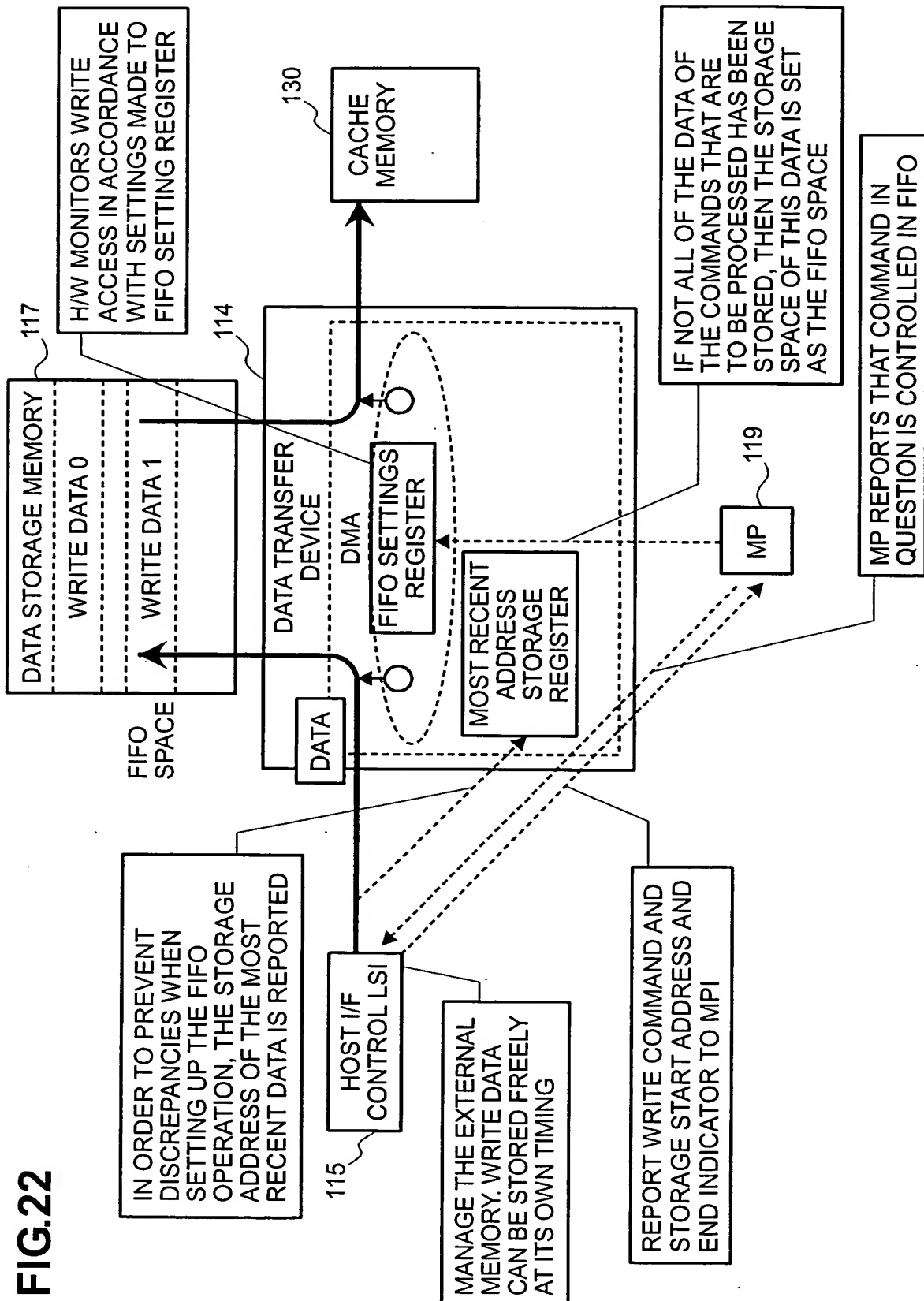


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FIG.22

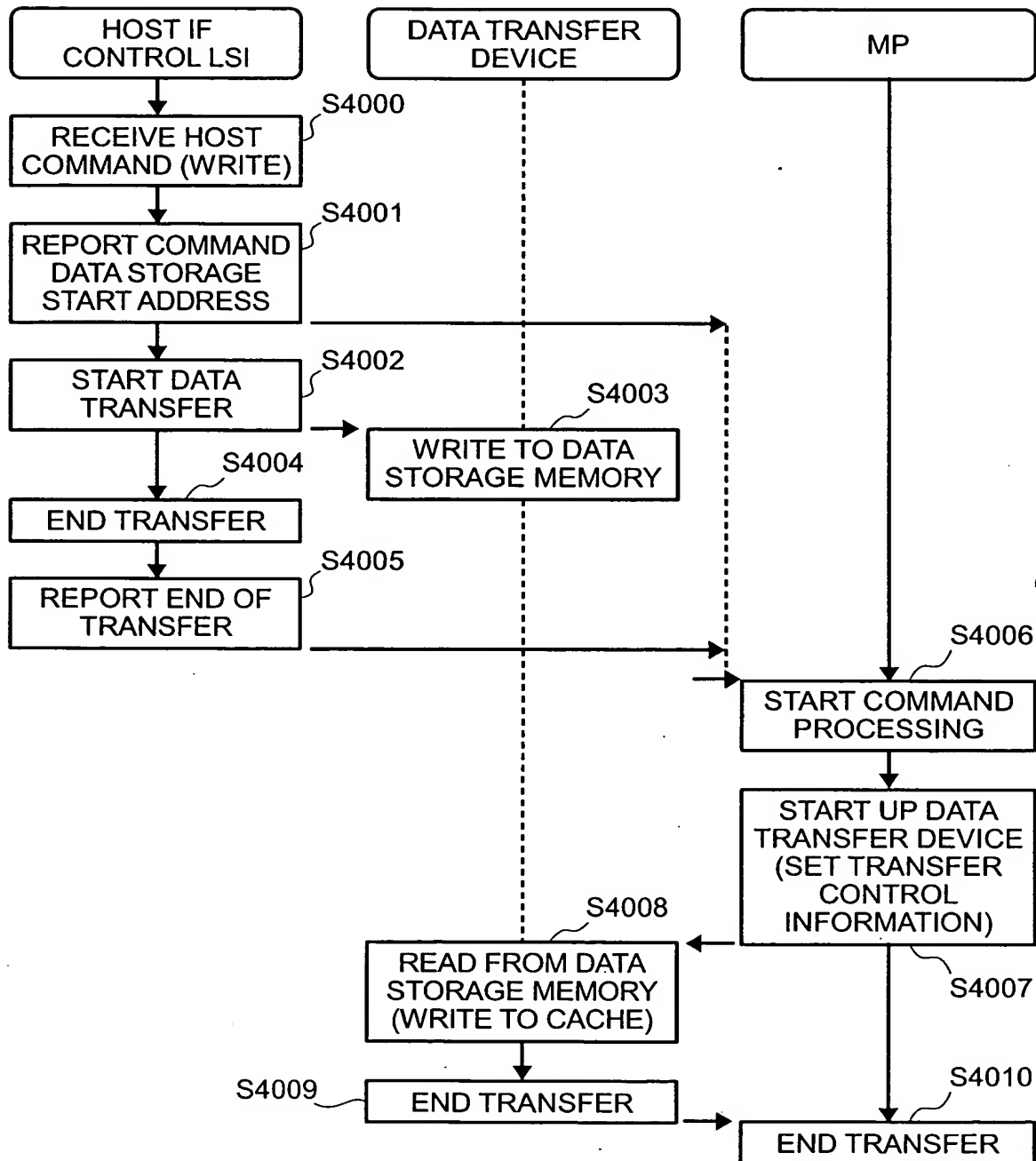
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FIG.23

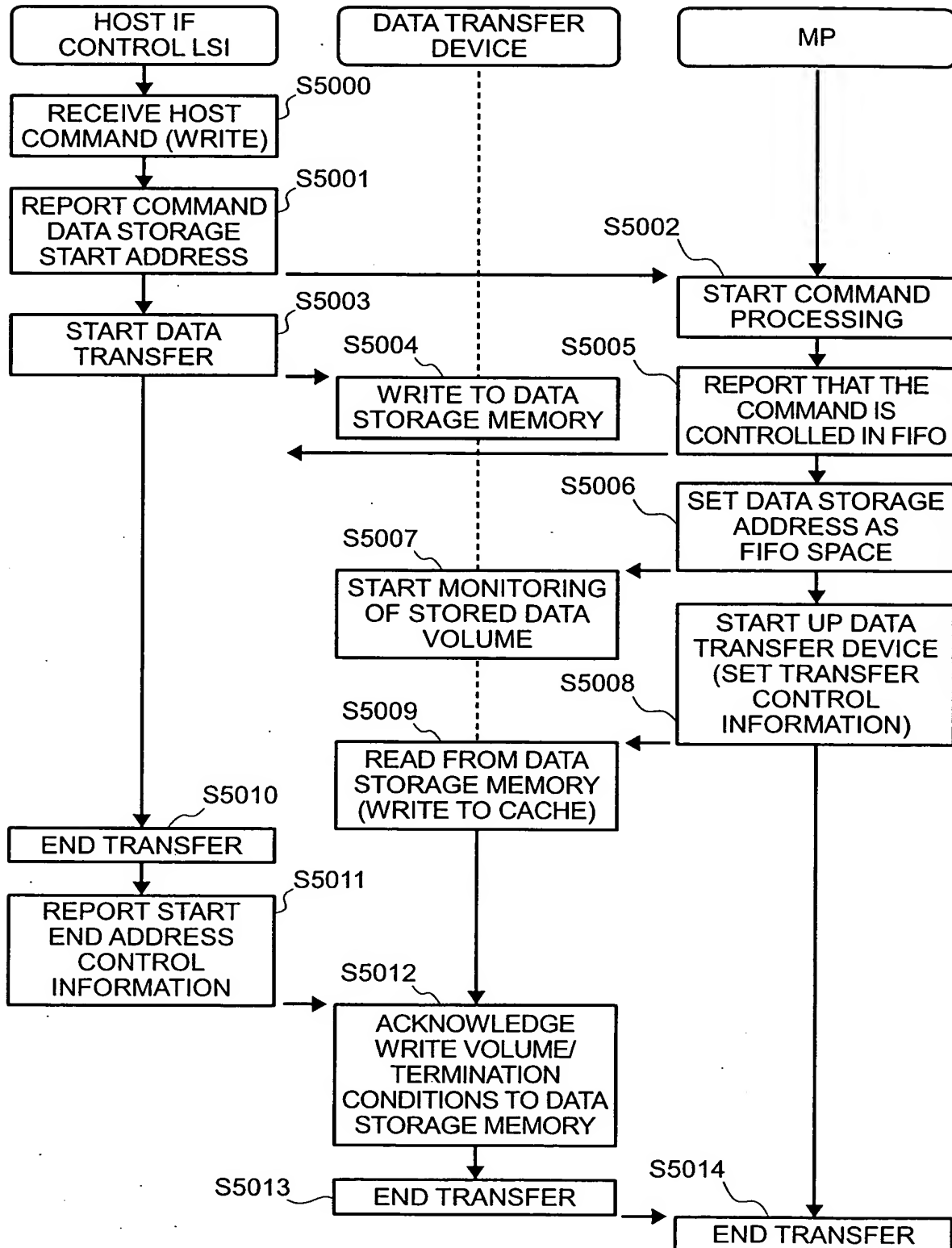


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FIG.24

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FIG.25

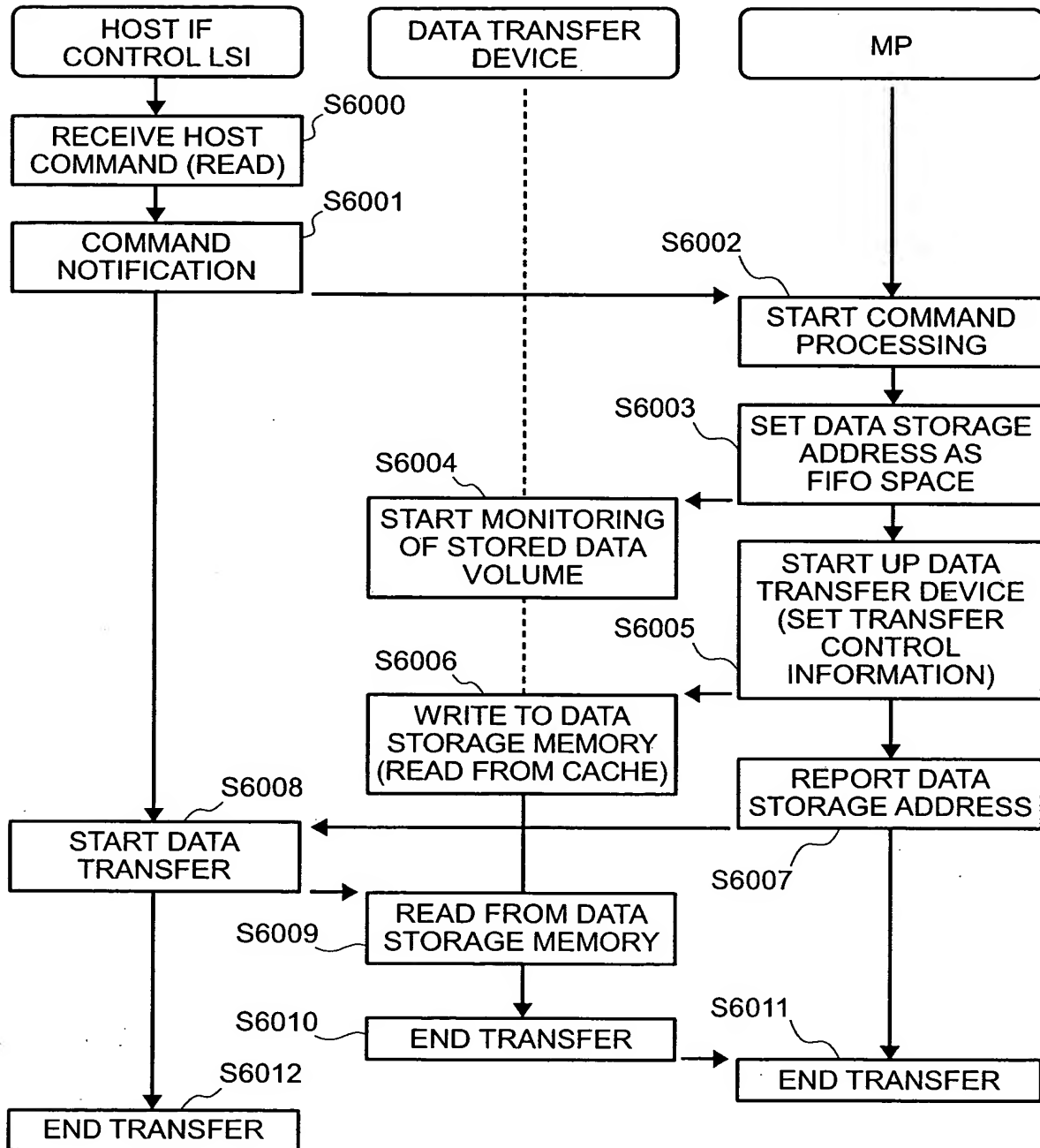


FIG. 26

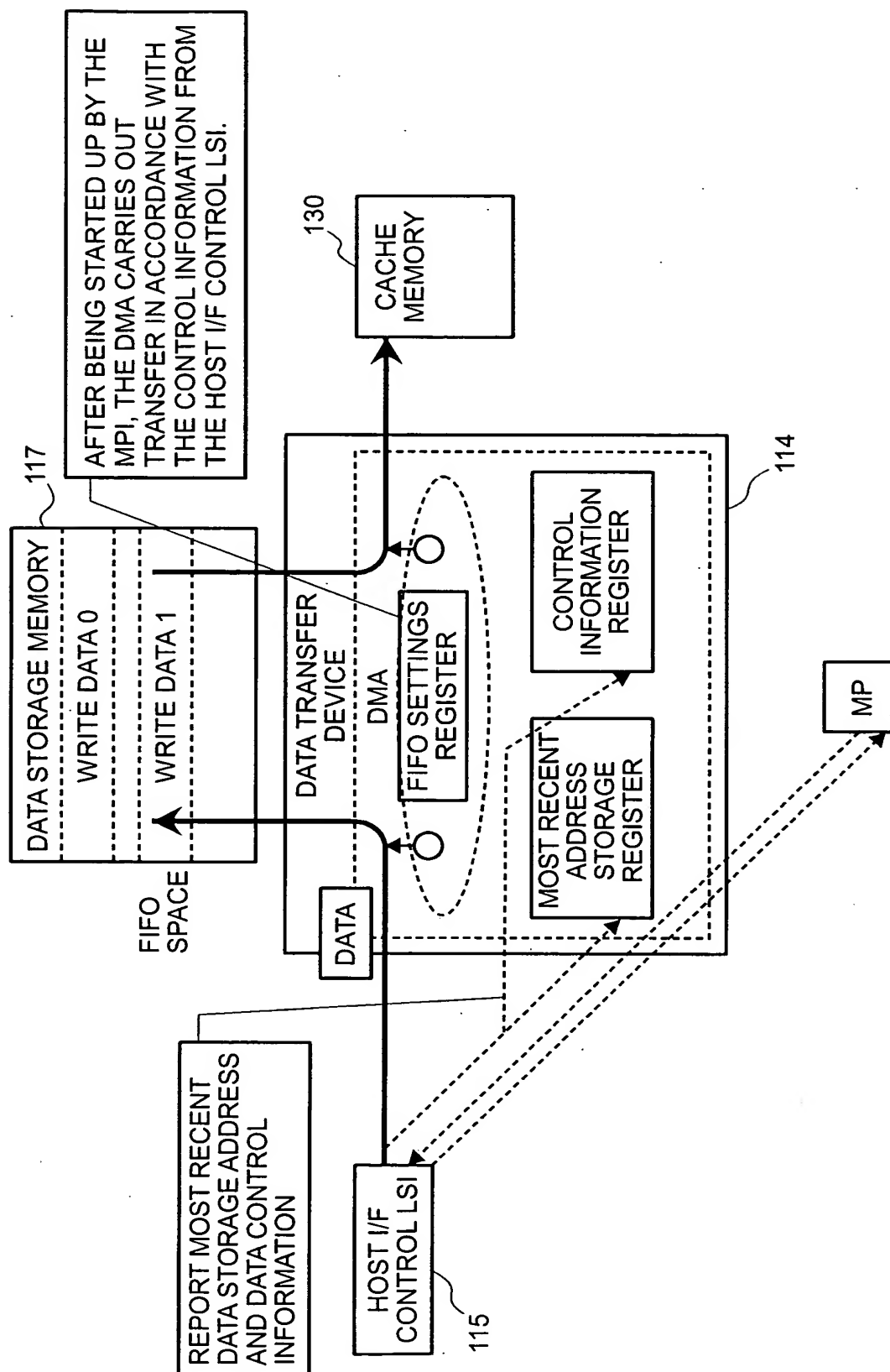


FIG.27